Xilinx Products, Solutions and Technology for ADAS/AD

Paul Zoratti
Xilinx
Director: Automotive Solutions & Architects

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Xilinx Product Evolution in Automotive

- **FPGA**
  - 1 Mpixel Camera Warning (only)
  - Bird's Eye View

- **HW Programmable SoC**
  - 2 Mpixel Camera Warning & Mitigation
  - 3D Surround View

- **HW Programmable MPSoC**
  - 4 Mpixel Camera Broader Protection & Control
  - Dynamic 3D Surround

- **ADAPTIVE COMPUTE ACCELERATION PLATFORM**
  - 8 Mpixel Camera Autonomous Drive/Park
  - Next Gen 3D Surround w/ AI

Timeline:
- 2008: 1 Mpixel Camera Warning (only)
- 2010: 2 Mpixel Camera Warning & Mitigation
- 2012: 3D Surround View
- 2014: Dynamic 3D Surround
- 2016: Broader Protection & Control
- 2018: Next Gen 3D Surround w/ AI
- 2020: Autonomous Drive/Park
- 2022: Adaptive Compute Acceleration Platform
Xilinx All Programmable SoC and MPSoC
A Game Changing Technology in Automotive
Xilinx Automotive SoC & ACAP Applications

Scalable Family of Automotive Targeted Devices

16 nm

~2 to ~200 Acceleration TOPs (INT8, nearly 400 TOPs at INT4)

Radar/Lidar

Driver Monitoring

In Cabin Monitoring

Fwd Camera

Radar/Lidar

Understanding AD Processing “Roles”

Zynq Processing Roles

ZU+ Processing Roles

Versal Processing Roles

DAPD = Data Aggregation, Pre-Processing & Distribution

Accel = Compute Acceleration (e.g. CNN Processing)

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Field Programmable Gate Array Based SoC’s

What is an FPGA?

Flexibility and Performance
Field Programmable Gate Array Based SoC’s

FPGA Fabric = Programmable Logic

- Common Processor Peripherals (e.g. CAN / CAN-FD)
- MicroBlaze 32-bit Soft Processor
- Application Focused Connectivity (e.g. MIPI CSI-2 Controller and D-PHY)
- Highly Parallelized and Customized DSP Acceleration (e.g. FFT)
- Inference DNN Processing Engines
- Unique, Differentiating User-Defined Functions or Pipelines of Functions

MicroBlaze 32-bit Soft Processor

Common Processor Peripherals
(e.g. CAN / CAN-FD)

Application Focused Connectivity
(e.g. MIPI CSI-2 Controller and D-PHY)

Highly Parallelized and Customized DSP Acceleration (e.g. FFT)

Inference DNN Processing Engines

Unique, Differentiating User-Defined Functions or Pipelines of Functions

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Functional Partitioning for Zynq UltraScale+
A Heterogenous Processing Platform

- HMI Graphic Overlay
- Configuration Security Unit
- Platform Management Unit
- System Control Decisions
- Diagnostics / FuncSafety
- Vehicle Comms

- Feature Application SW
- Algorithm Configuration & Control
- Object Tracking
- Environment Assessment
- Feature State Control

- Parallelized Computational Accelerators
- High Bandwidth Large Volume Data
- Scalable/Adaptable Interfaces
- Application Specific FS Circuits/Monitoring

Functional Safety Elements
ASIL Support

Sensor / HMI Interfaces
(e.g. MIPI CSI-2 / DPHY)

Video Processing
(Pixel Manipulation)

Image Analytics
/Machine Learning Acceleration

ToF (Radar/Lidar)
Sensor Processing

Sensor Fusion & Perception Acceleration
Versal Architecture Overview

Adaptable Engines
- 2X compute density
- Voltage scaling for perf/watt

Scalar Engines
- Platform Control
- Embedded Edge Compute

PCle Gen4/5 & CCIX
- 2X PCIe & DMA bandwidth
- Cache-coherency

DDR4 Memory
- 3200-DDR4, 4266-LPDDR4
- 2X bandwidth/pin

Transceiver Leadership
- Broad range, 1G →112G
- 58G in mainstream devices
- (32G in XA)

Intelligent Engines (DSP)
- AI Compute
- Diverse DSP Workloads

Programmable NoC
- Guaranteed Bandwidth
- Enables SW Programmability

Programmable I/O
- Any interface or sensor
- Includes 3.2Gb/s MIPI
Forward-Looking Camera Partitioning Example

Actuation ECUs
- Braking
- Steering
- Throttle
- Suspension etc

HMI ECUs
- Displays
- User Input
- Driver Monitor

Radar/Lidar Sensor(s)

CAN / CAN-FD / Ethernet PHYs

Scalar Engines
- Cortex-A72’s
  - Feature Application SW
  - Algorithm Config & Ctrl
  - Object Tracking
  - Environment Assessment

Adaptable Engines
- Sensor Fusion Accelerators
- ML Data Conditioning and Buffering
- Computer Vision Processing Accelerators
- Custom Optimized and Scaleable ISP

Intelligent Engines
- AI ENGINES
  - ML Computational Processing (e.g. CNN)
- ISP Acceleration and/or Stereo Disparity

Forward Camera Module

Optional Stereo

PCiS & CCIX
- DDR
- HBM
- SerDes
- Network Cores
- MPI
- LVDS
- GPIO

Actuation ECUs

HMI ECUs

Radar/Lidar Sensor(s)
ML Processing on Versal
DPU Architecture Design

- Target: Configurable/Scalable DPU
  - DPU = Deep-learning Processing Unit
  - A powerful combination of PL and AIE resources to realize optimized ML Processing

- AIE: Conv engine

- PL: Depthwise Conv, Elementwise, Pooling, softmax and Instruction scheduler

- Instruction: Control the data flow between AIE and PL. Control different engines in MISC.
Xilinx Solutions Slides
From horizontal IP to partner application specific solutions
Demo specification

- Model: Pointpillars
- Framework: Pytorch
- Dataset: Kitti, 64-channel, 1~2Mpoints/sec
- 25fps (40ms latency), 1x DPU B4096 @ 300MHz on ZCU102
- General access in Vitis AI 1.3
ZU+ -based 4D Radar Processor Concept
Hardware Accelerated Performance Optimized to RF Modulation and Control Strategies

**Processing System**
- **High Speed**
  - Display Port
  - USB 3.0
  - SATA 3.0
  - PCIe Gen2
  - PCI-Express
- **Real-Time Processing**
  - Quad ARM Cortex™-A53
  - ARM Mali™-400 MP
  - Memory Management Unit
  - 32KB L1 Cache with ECC
- **Security**
  - AES Decryption, Authentication and Secure Boot
- **Platform Management**
  - Power
  - System Management
  - DMA, Timers, WDT, Reboots, Clocking and Debug

**Programmable Logic**
- System Gates, DSP, RAM
- Functional Safety Support
  - (e.g. Cross Monitoring, Voting, Watchdog)
- RF/Sensor Control Logic/State Machine
- Object Detection Accelerator
- Object Tracking Accelerator
- Doppler FFT
- Frame Based Processing
  - Pulse Integration, Detection, Range Rate, & Tracking

**Digital Beamforming**
- Azimuth/Elevation Processing
  - Phase Differences

**FFT Input Conditioning & Buffering**
- Complex Streaming FFT
- FFT Output Conditioning & Buffering

**Pulsed Based Range Processing**
- Streaming data from multiple antenna elements

**RF AFE**
- MIPI

**Comms, Diagnostics, Watchdog Code**
- Sensor Application Code
- Comms, Diagnostics, Watchdog Code
- High Speed Multi-Channel A/D Converters

**Object Tracking Accelerator**

**RF/Control Components**
- Beam Element/Motor Control Integration

**Functional Safety Support**
(e.g. Cross Monitoring, Voting, Watchdog)

**PROTECTED. CUSTOMIZED. DIFFERENTIATING, AND PRODUCT SPECIFIC IP OPPORTUNITIES**

**Processing System**
- DDR
- DDR Controller
- 256KB OCM with ECC

**Multi Channel Data Capture**
- FFT Input Conditioning & Buffering
- Complex Streaming FFT
- FFT Output Conditioning & Buffering

**Digital Beamforming**
- Azimuth/Elevation Processing
  - Phase Differencing Between Elements

**RF/Control Components**
- Beam Element/Motor Control Integration

**RF/Control Components**
- RF/Control Components

**RF/Control Components**
- RF/Control Components
Viewable System Processing

- From simple rear view camera to mirror enhancement and replacement to 3D surround view with flying camera

- Image Warping, Stitching (Panoramic, Bowl, other), and View Transformation in a scalable product family to cost effectively meet sensor and system performance needs

- Full development platform available from Xilinx Ecosystem Partner Xylon
Vision Analytics Processing

- From traditional machine vision to the latest and innovative ML vision processing
- A new breed of Xilinx Ecosystem Partner
Automated Parking Functionality as Foundation for Domain Controller and other AD initiatives

> Combining Surround View, ML Processing and Vehicle Control into an automated parking feature
Some Xilinx Sourced Relevant IP

- **Connectivity**
  - MIPI CSI, MIPI DSI, HDMI, Display Port
  - Ethernet TSN, SLVS

- **Video Processing**
  - Mixer, Scaler, Framebuffer, Video Controller
  - ISP – DPC, Demosaic, Gamma Correction, AWB/AE, HDR, Color Correction, Noise Reduction, etc.
  - Transformation, Image Warping and Stitching

- **Image Processing**
  - OpenCV Libraries – e.g. Harris Corner, Optical Flow, Stereo Disparity, HoG/SVM, Hough Transform

- **General**
  - Windowing, FFT, Kalman Filter, SVD, FIR Filter, etc.
Xilinx Unique Technology Advantages

OTA HW
Dynamic Function Exchange
Functional Safety
Over-the-Air Silicon Updates (OTA)

- Over-The-Air update to enable modifications for Software AND Hardware
- Evolve neural network implementations over time
- Add new features or update mission critical functions
- Future proof for emerging security threats
- Update safety algorithms
- Perform remediation or corrective action

Upgrade Hardware of Deployed Systems
Dynamic Function eXchange (DFX)
Efficient, Low Latency Exchange of Functions

- Leverages the ability to reprogram portions of Xilinx Programmable Logic (PL) fabric while the remainder of the fabric remains fully functional

- Result is “silicon re-use” for uniquely efficient, cost-effective implementation of mutually exclusive applications
Example Multi-Feature Sensor Configuration
### Mutually Exclusive Feature Bundles

<table>
<thead>
<tr>
<th>Pre-Drive Security</th>
<th>Low-Speed/Parking</th>
<th>Highway Driving</th>
</tr>
</thead>
<tbody>
<tr>
<td>Keyless Entry</td>
<td>Automated Park Assist</td>
<td>Driver Monitoring System</td>
</tr>
<tr>
<td>Vehicle Security</td>
<td>360 Degree Surround View</td>
<td>Forward Camera w/ Surround Monitor</td>
</tr>
<tr>
<td>Biometric Identification</td>
<td></td>
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Central Module Architecture

- **Display ECU’s**: MIPI CSI-2 / DPHY Controller
- **Vehicle Status/Control Bus**: CAN / CAN-FD PHY, 100Mb/1Gb Ethernet PHY, DeBug/Devel Port(s), Non-Volatile FLASH Device(s) (bitstreams), US ASIC
- **Ultra sonics**: 100Mb/1Gb PHYs/Switch
- **DMAs for MIPI/Ethernet Interfaces**: Ethernet MAC (TSN or could leverage hardened MAC), MIPI CSI-2 / DPHY Controller
- **Functional Safety Elements ASIL Support**: Radar/Lidar, Surround Cams, Internal Cams, Forward Cams

Sensor Data Available to Reconfigurable PL space either thru direct connection to interface blocks for from DDR memory buffers.
Central Module Architecture

- **Vehicle Status/Control Bus**: CAN / CAN-FD PHY, DeBug/Devel Port(s)
- **Display ECU’s**: 100Mb/1Gb Ethernet PHY (Incl BR), Non-Volatile FLASH Device(s)
- **Ultra sonics**: US ASIC
- **Radar/Lidar**: Quad SERDES
- **Surround Cams**: MIPI CSI-2 / DPHY Controller, CSI-2 4-lane
- **Internal Cams**: MIPI CSI-2 / DPHY Controller, CSI-2 4-lane
- **Forward Cams**: MIPI CSI-2 / DPHY Controller, CSI-2 4-lane
- **DMAs for MIPI/Ethernet Interfaces**: Ethernet MAC (TSN or could leverage hardened MAC)
- **CAN-FD (Ultrasoundic Range Data)**
- **DDRC**
- **GPU**
- **A5x**
- **OCM**
- **Cache**
- **Reconfigurable PL**
- **Power Supply**
- **Output Video Formation & Control (Stitching/Blending, Overlay)**
- **Image Warp (Distortion Correction, Perspective Projection)**
- **Image Capture (4x)**
- **Image Scale**
- **Sensor Fusion**
- **Frame Sync**
- **Image Analytics / Machine Learning Acceleration**
- **Sensor Fusion & Perception Acceleration**
- **Video Processing (Pixel Manipulation)**
- **ToF (Radar/Lidar) Sensor Processing**
- **Functional Safety Elements ASIL Support**

**Low Speed/Parking**

- **Functional Safety Elements ASIL Support**

**Surround Cams**

- **100Mb/1Gb PHYs/Switch**
- **MIPI CSI-2 / DPHY Controller**
- **CSI-2 4-lane**
- **Dual SERDES**

**Internal Cams**

- **MIPI CSI-2 / DPHY Controller**
- **CSI-2 4-lane**
- **Dual SERDES**

**Forward Cams**

- **MIPI CSI-2 / DPHY Controller**
- **CSI-2 4-lane**
- **Dual SERDES**

- **DDRC**
- **GPU**
- **A5x**

- **Reconfigurable PL**

- **Output Video Formation & Control (Stitching/Blending, Overlay)**

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**Low Speed/Parking**
Dynamic Function eXchange (DFX)
Efficient, Low Latency Exchange of Functions

- Leverages the ability to reprogram portions of Xilinx Programmable Logic (PL) fabric while the remainder of the fabric remains fully functional.
- Result is “silicon re-use” for uniquely efficient, cost-effective implementation of mutually exclusive applications.
- Silicon Re-Use = Lower Density Device = Lower Cost & Power
Xilinx Functional Safety Solutions

- IPs & Methodologies
- Software
- Certification Authorities
- Reference Design & Ecosystem Partners
- Certified Development Tools
- SoC & FPGA

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Summary

- **Cost-effective & Scalable Device Families**
  - Platform design for BoM scaling to various ADAS / AD Sensor and Feature Bundles

- **Unique IP portability**
  - IP designs migrate to / from Distributed Sensors to Centralized Modules

- **Optimal Partitioning Between System Software and Hardware Accelerators**
  - Integrated Sensor Data Aggregation, Compute Acceleration, and Scalar Processing

- **Power Efficient, High Utilization AI / ML Inference**
  - More effective use of TOPs

- **Customer-owned (Proprietary) or Xilinx / Partner Licensable IP / Accelerators**
  - Market Differentiation / Leadership and Fast Time to Market

- **Independent (Isolated), Simultaneous, and Optimized Processing Pipelines**
  - Lowest latency sensor data paths and sensor fusion

- **In-field SW and HW upgradability (Unique OTA-HW)**
  - Unparalleled ability to update system capabilities / performance

- **Dynamic Function Exchange (processing pipelines) for Unmatched Adaptability**
  - Efficiently address multi-feature systems requirements with minimized cost & power
Thank You